Designing of a 10MHz BW 77dB SNDR 8.1mW Continuous-Time Delta-Sigma Modulator With a Proposed Low Power, Rail-to-Rail Output Swing OPAMP

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Matsuzawa & Okada Lab.

Outline

- Background
- Design target
- Proposed OPAMP
- Block circuits design
- Simulated performance
- Conclusion

Background

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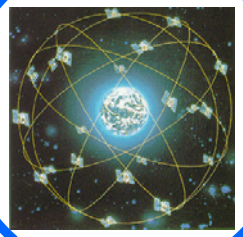
Ultimate terminal

Mobile Phone

TV

Satellite



Telephone call

DTV

FM

GPS

Terminal

Bluetooth

RFID

WLAN

UWB

PC

digital consumer electronics

POS

Software Defined Radio (SDR)

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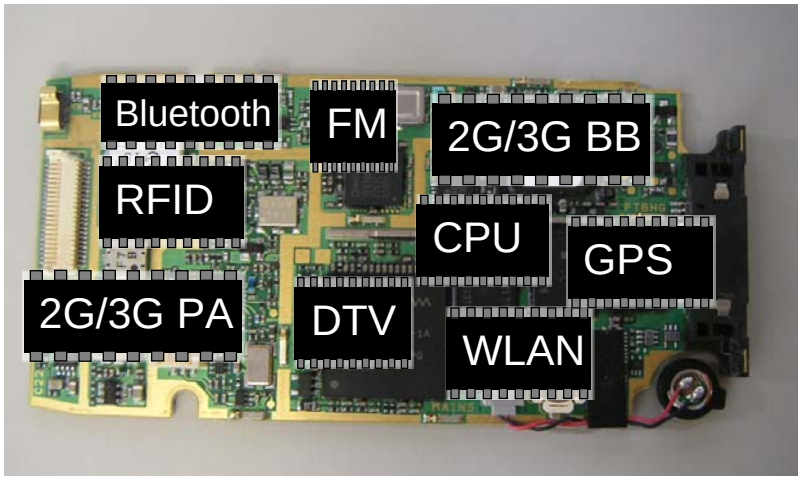
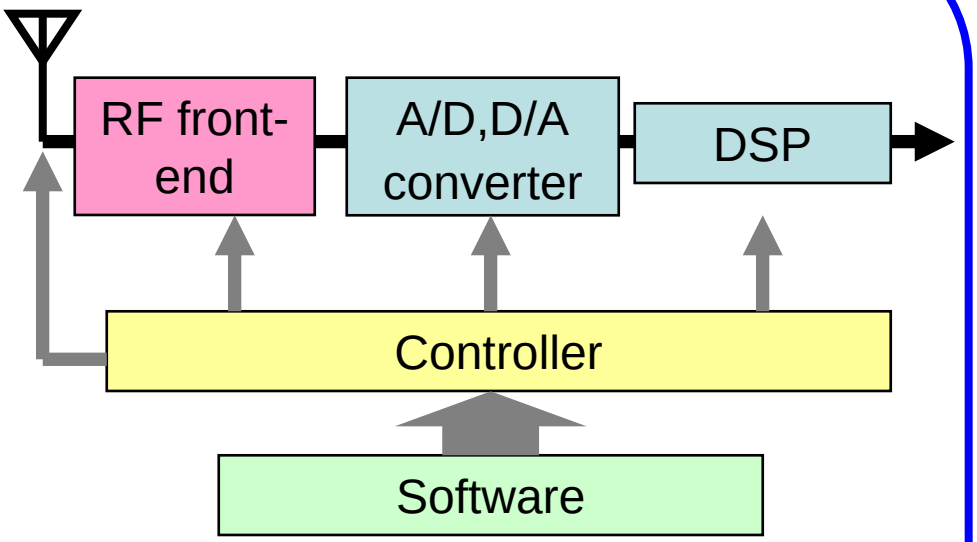
Current



Future

＜Software Defined Radio＞



Compliant with multi standard

ADC for multi-band RF front-end is needed

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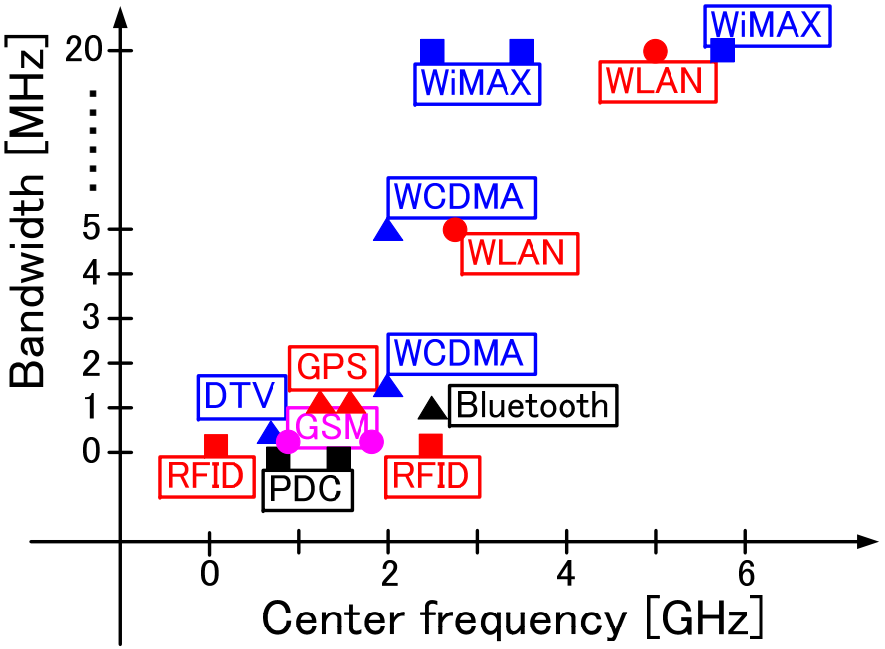
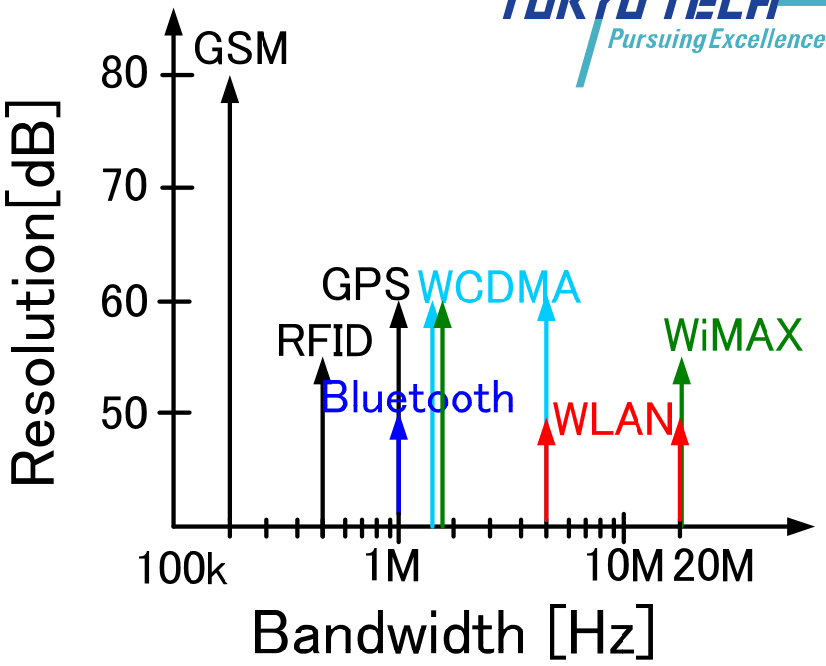
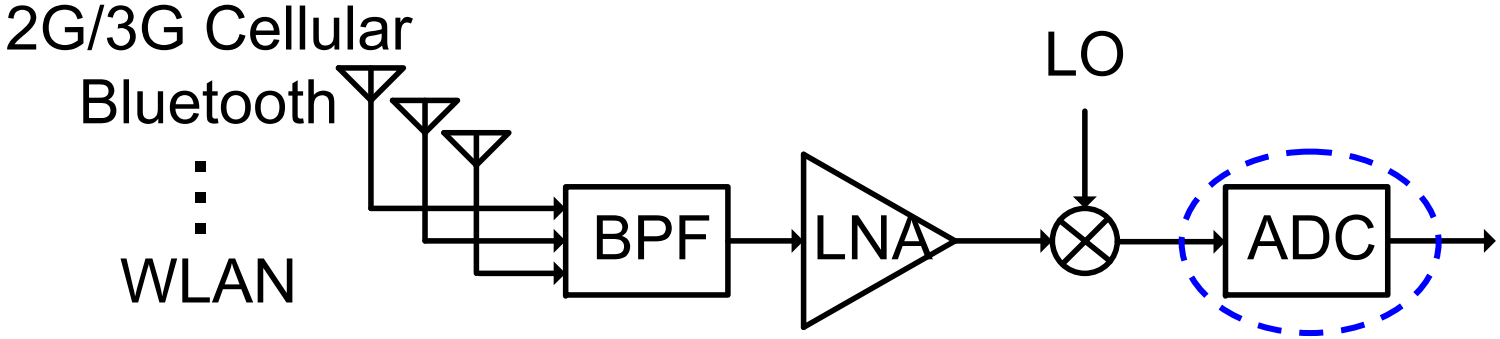
SDR Requirement



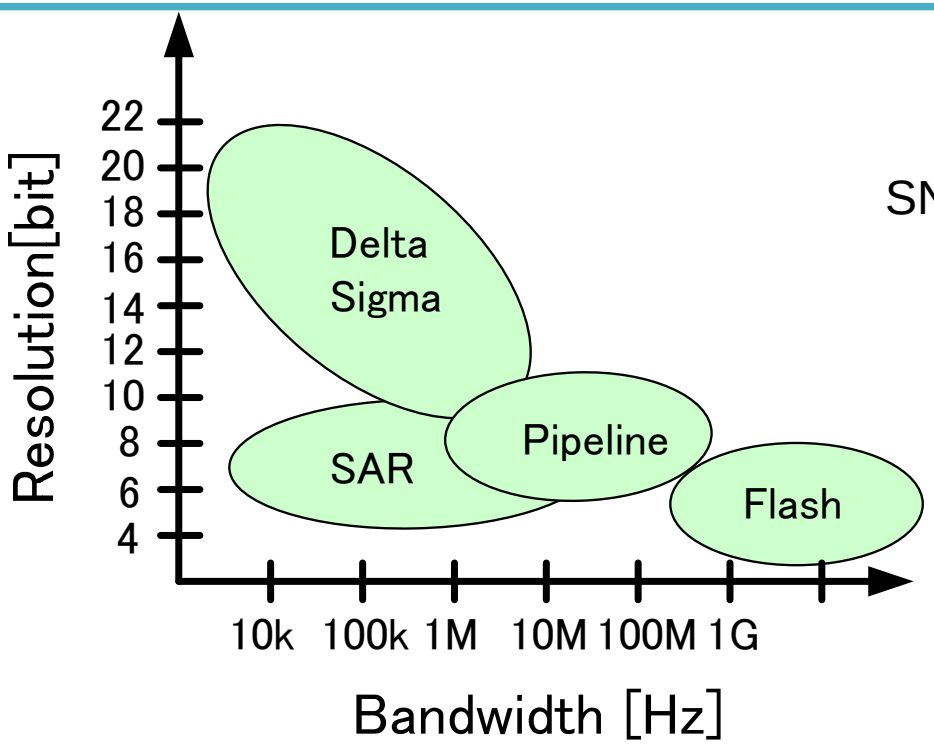




*A reconfigurable wide band, high resolution ADC

*Smaller size, lower power

ADC performance



SNDR [dB] = 6.02*bit + 1.76

Type	Conversion frequency	Resolution	Power
Flash	○	×	△
Pipeline	△	△	△
SAR	×	△	○
ΣΔ	×	○	△

ΔΣ ADC is a hopeful solution for SDR

Design target

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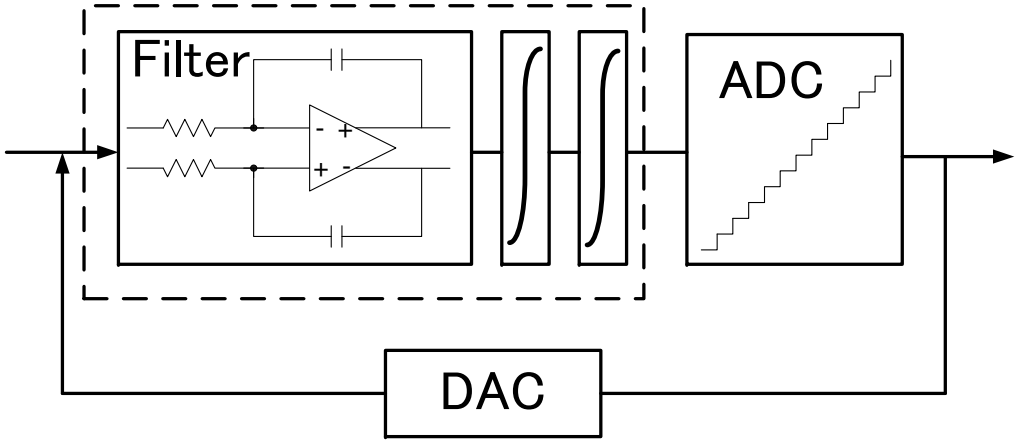
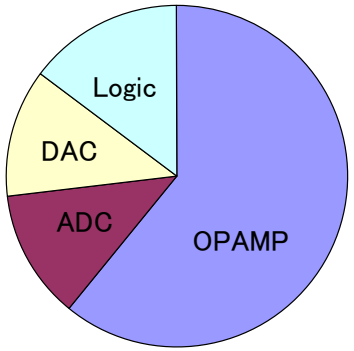
Bandwidth	10MHz (Final: configurable)
Sampling frequency	320MHz
Resolution	75dB (Final: configurable)
Input range	1.6V diff
Supply voltage	1.2V
Power consumption	~8mW (Final: configurable)
Area	~0.5 mm^2
Process	90nm CMOS process
Figure of Merit (Smaller FoM is better)	<100fJ/conv

A reconfigurable wide band, high resolution ADC will be developed in the future, and not be told in this presentation.

ΔΣ modulator architecture



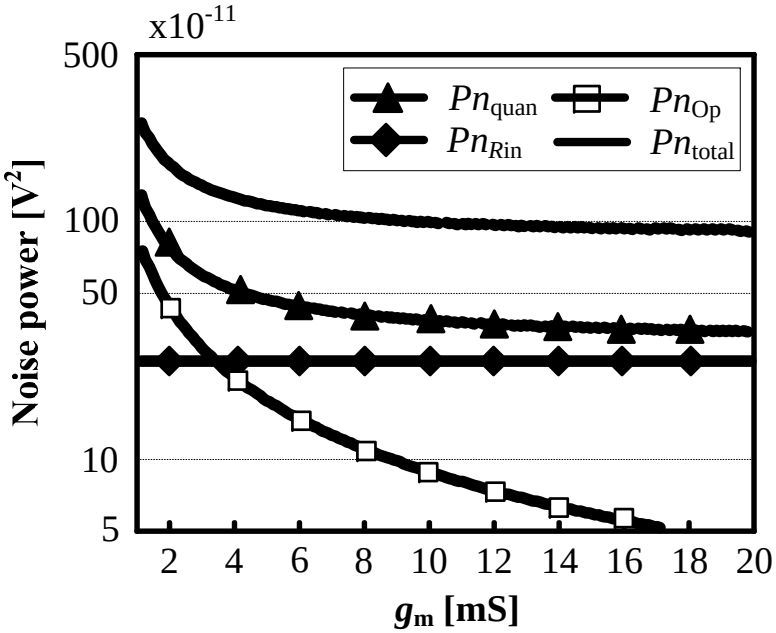
Power contribution



Low g_m in an OPAMP
→ OPAMP noise increase
→ Total noise increase
→ Resolution decrease

Low power, low noise OPAMP is required

Noise contribution



Conventional OPAMP

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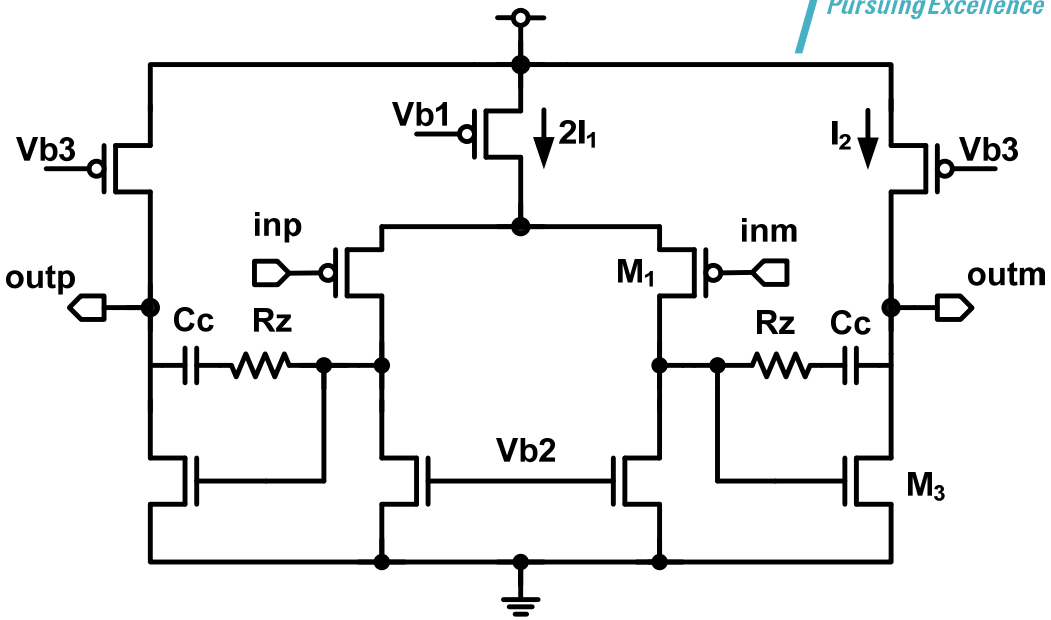
- Single-stage opamps
  - Power effective
  - No rail-to-rail output
  - Low gain
- Two-stage opamps
  - Ineffective power consumption
  - Rail-to-rail output
  - High gain



$$A = g_{m1} \cdot r_{o1} \cdot g_{m3} \cdot r_{o3}$$

$$g_{m1} = \frac{2 \cdot I_1}{V_{eff}} \qquad g_{m3} = \frac{2 \cdot I_2}{V_{eff}}$$

$$GBW = \frac{g_{m1}}{2\pi \cdot C_C}$$

(V_{eff}: override voltage)

Key idea : increase g_m/I

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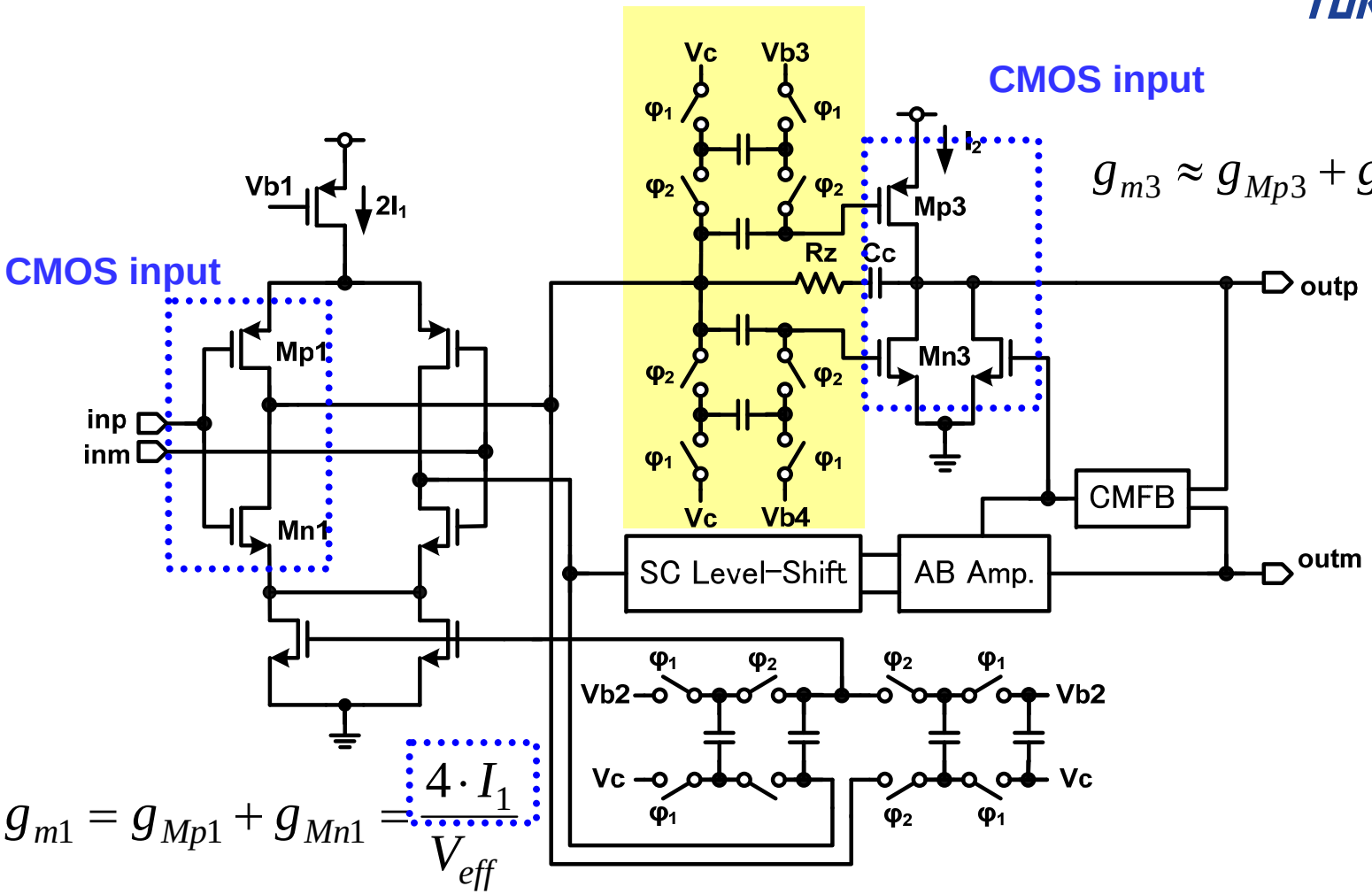
Proposed OPAMP



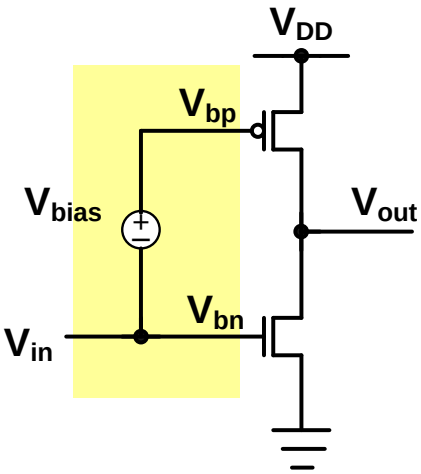
$$g_{m3} \approx g_{Mp3} + g_{Mn3} = \frac{4 \cdot I_2}{V_{eff}}$$

$$g_{m1} = g_{Mp1} + g_{Mn1} = \frac{4 \cdot I_1}{V_{eff}}$$

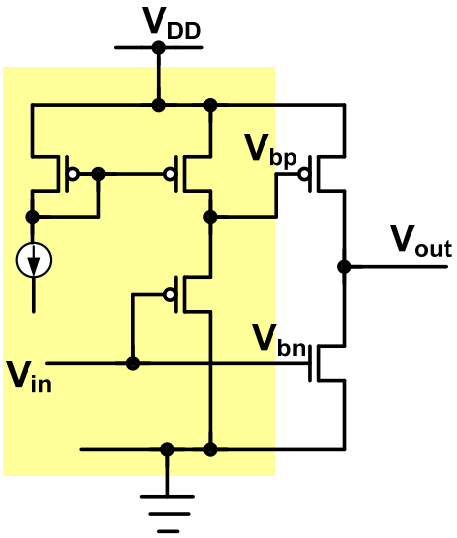
***A rail-to-rail, high power-efficient opamp**

***Using SC level shifter in continuous-time integrator**

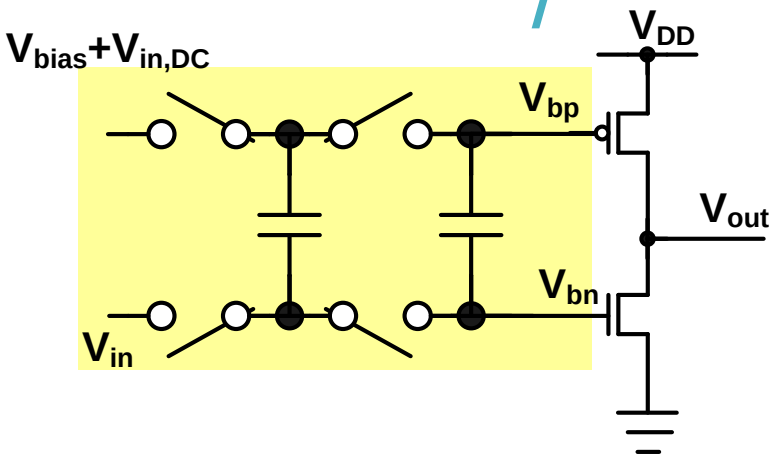
Merit of SC-level shifter (SCLS)



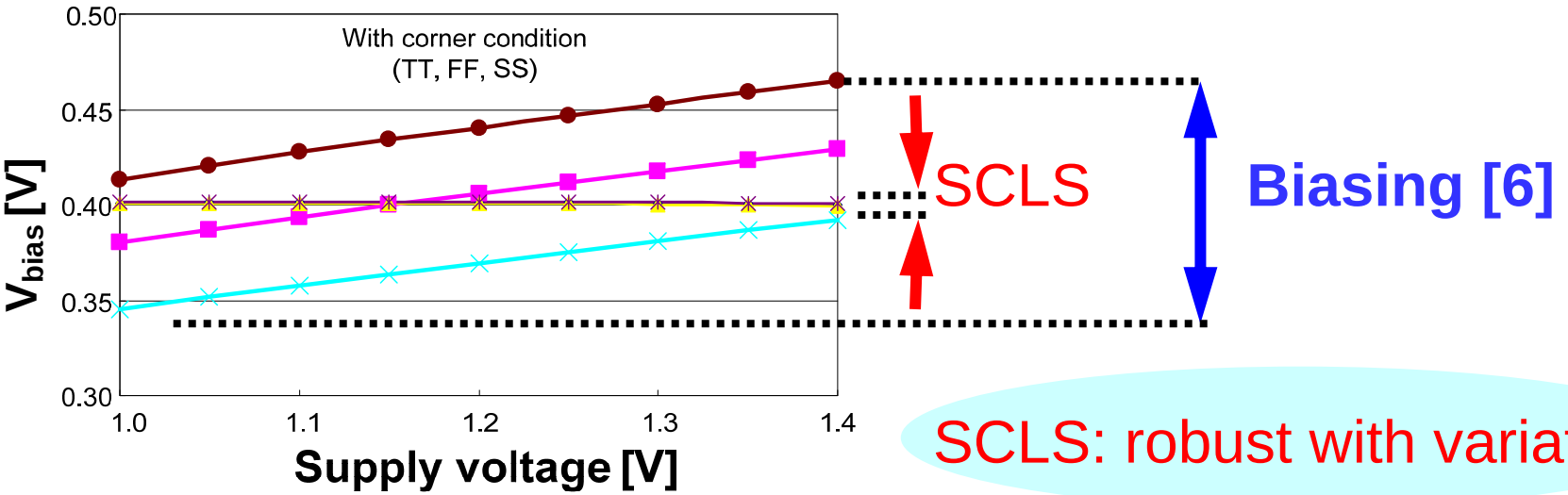
Class-AB



Class-AB biasing[6]



Class-AB biasing(SCLS)



SCLS: robust with variation

Noise consideration

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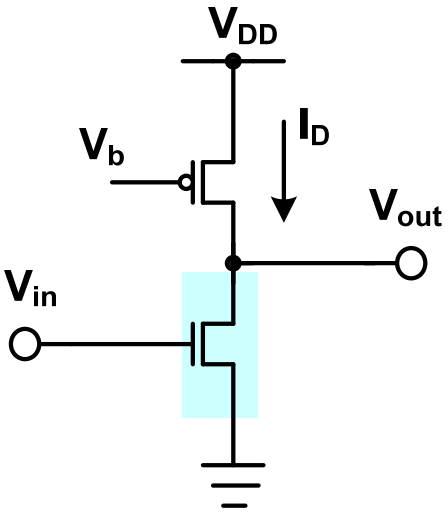
Noise figure of merit: $$FoM_{noise} = \frac{1}{4kT}\overline{v_{n,in}^2} I_D$$

Same I_D

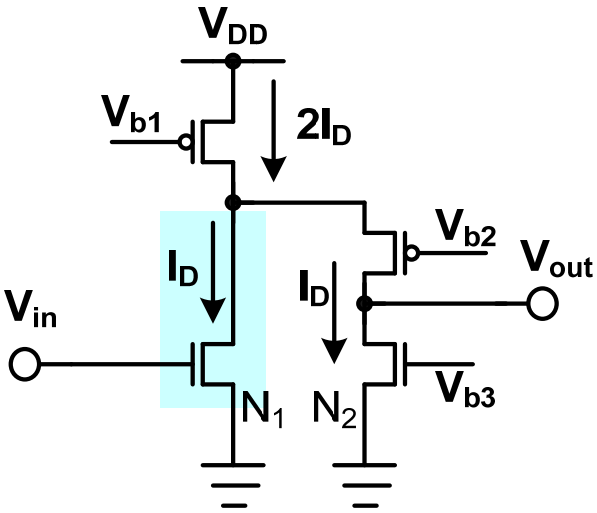


Common source

$$\overline{v_{n,in}^2} \approx 2 \times \frac{4kT\gamma}{g_{mn}}$$

$$FoM_{noise} = \frac{1}{4kT} \cdot 2 \times \frac{4kT\gamma}{g_{mn}} \cdot I_D$$

$$= \gamma V_{eff}$$

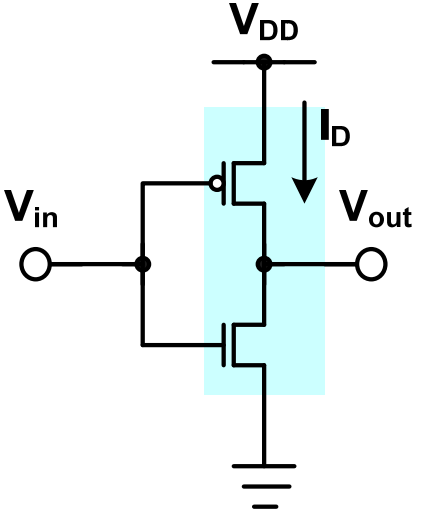


Folded-cascode

$$\overline{v_{n,in}^2} \approx 4 \times \frac{4kT\gamma}{g_{mn}}$$

$$FoM_{noise} = \frac{1}{4kT} \cdot 4 \times \frac{4kT\gamma}{g_{mn}} \cdot I_D$$

$$= 2\gamma V_{eff}$$



Complimentary input

$$\overline{v_{n,in}^2} \approx \frac{1}{2} \times \frac{4kT\gamma}{g_{mn}}$$

$$FoM_{noise} = \frac{1}{4kT} \cdot \frac{1}{2} \times \frac{4kT\gamma}{g_{mn}} \cdot I_D$$

$$= \frac{1}{4}\gamma V_{eff}$$

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OPAMP comparison (power)

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	Telescopic	Folded-cascode	2-stage (conv.)	Proposed
Supply voltage [V]	1.2			
Load	5.2pF//3.75kΩ			
DC Gain [dB]	36	37	51	55
Gain bandwidth [MHz]	700			
Phase margin [deg]	85	69.8	60	68
Output Swing [Vpp]	0.7	1	1.2	1.2
Power consumption [mW]	5.3	10.5	2.6	1.8

The proposed OPAMP consumes lowest power, save at least **30%** power when compared with the conventional 2-stage OPAMP

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OPAMP comparison (noise)

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	Telescopic	Folded-cascode	2-stage (conv.)	Proposed
Supply voltage [V]	1.2			
Load	5.2pF//3.75kΩ			
DC Gain [dB]	22	22	51	55
Gain bandwidth [MHz]	100	110	420	700
Input referred noise @1MHz [nV/sqrt(Hz)]	7.5	9.3	7.7	3.8
Power consumption [mW]	0.8	0.8	0.8	0.8
	–	0.8	1	1
$\frac{FoM_{noise}(\text{conv.})}{FoM_{noise}(\text{proposed})}$	3.9	6.0	4.1	1

The proposed OPAMP shows the best noise performance, down to at least **25%** when compared with the conventional 2-stage OPAMP

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Outline

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- Background
- Design target
- Proposed OPAMP
- Block circuits design
- Simulation Performance
- Conclusion

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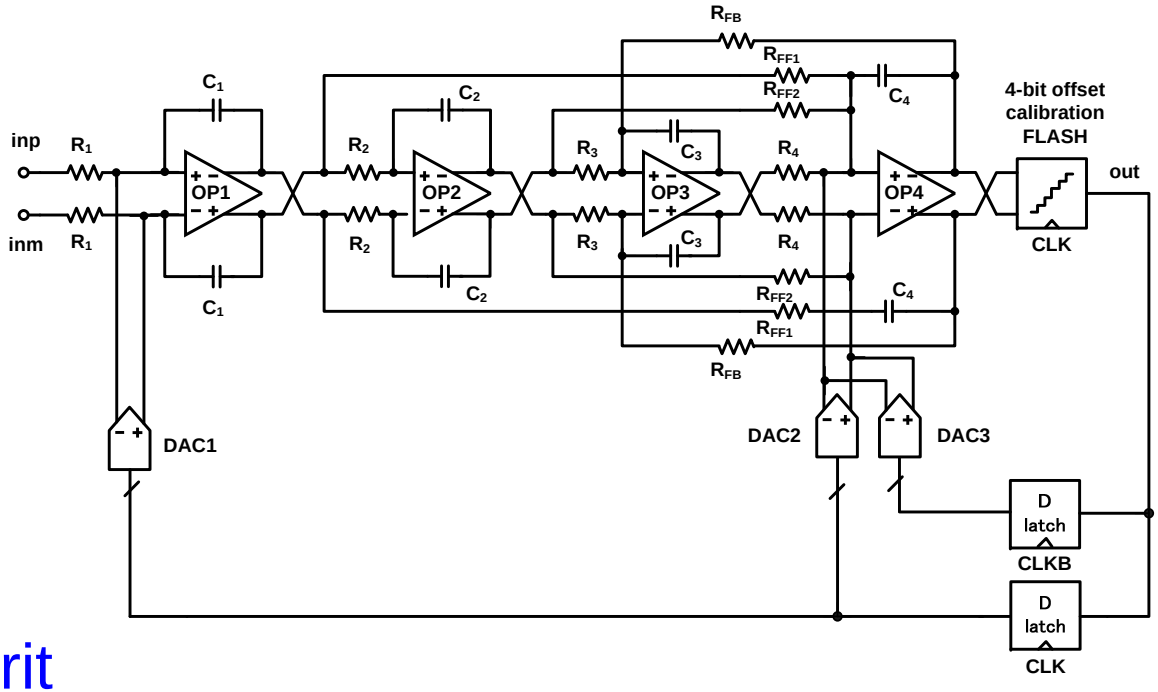
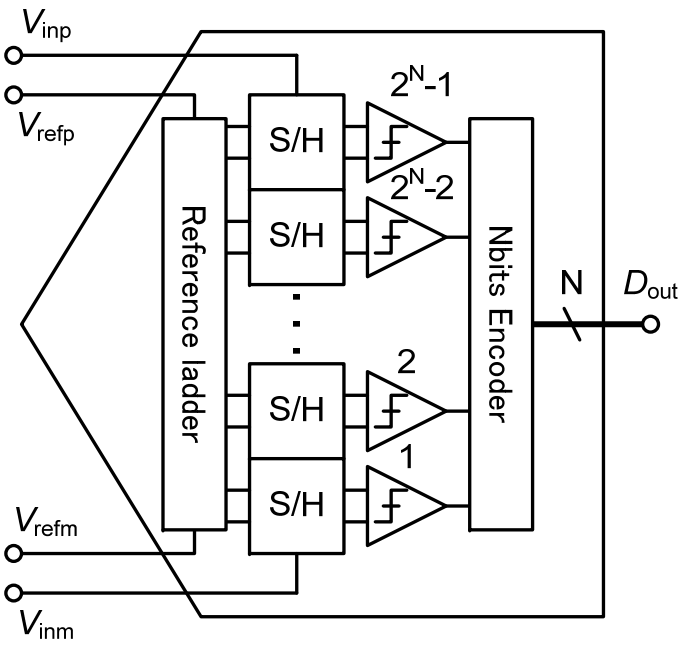
Modulator architecture

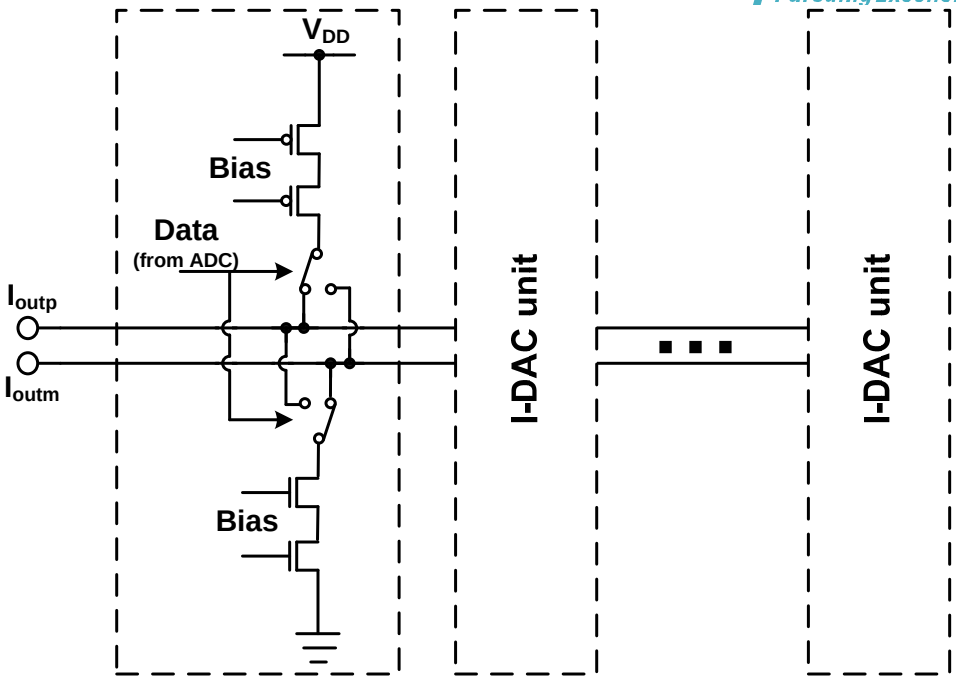


- Merit
  - Relax OPAMP output swing
  - Anti-alias characteristic
- Demerit
  - Need summing circuit before the ADC

    →Be shifted by applying the technique in [3]

ADC/DAC architecture





4bit Flash ADC

Dynamic comparator for low power consumption [7]

Offset calibration

Current-steering DAC

Non-return-to-zero DAC

Large device size to get the necessary matching and linearity

DEM (Dynamic element matching)

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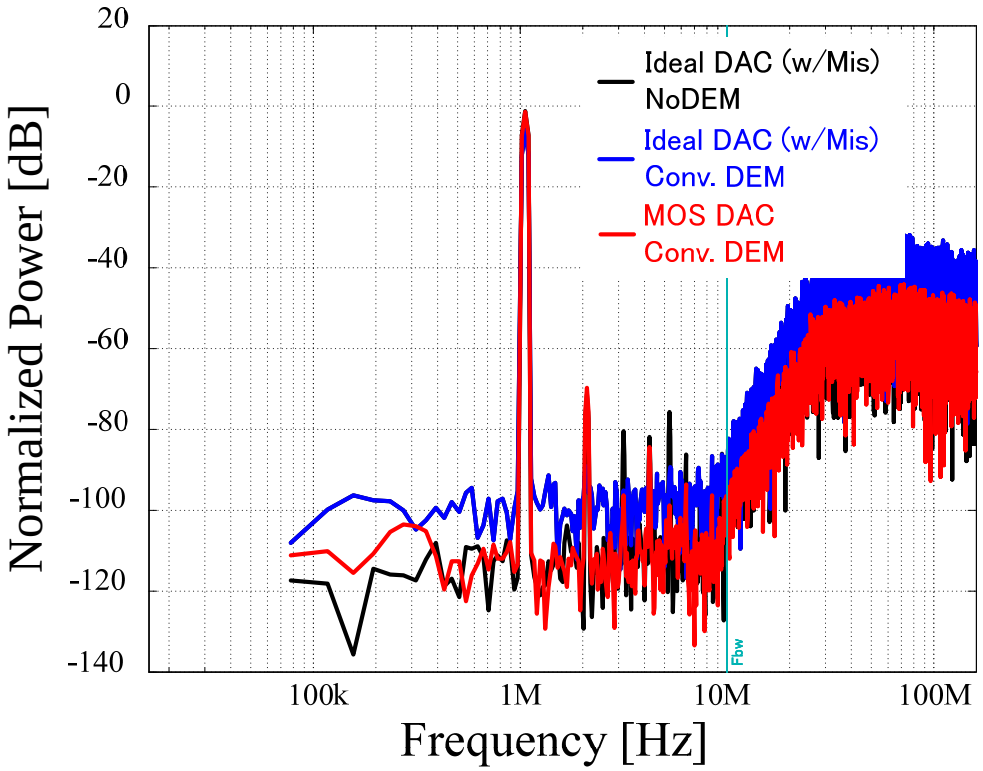
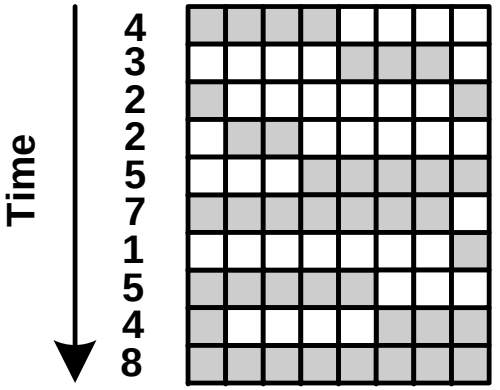
Merit: Better DAC linearity performance

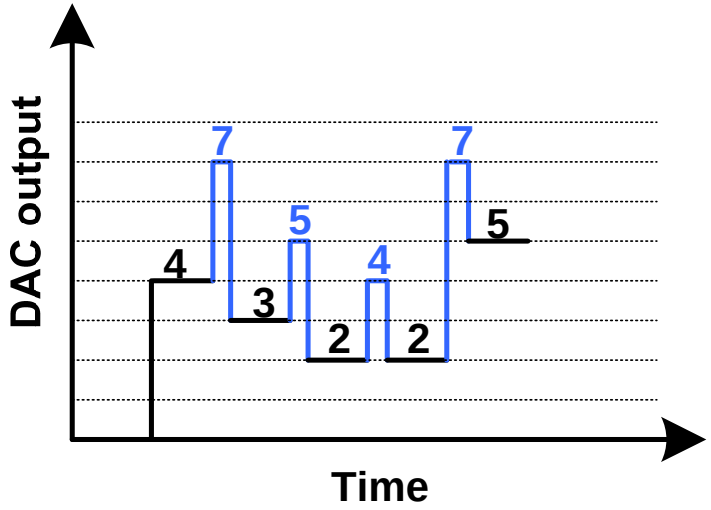
Issue: DEM delay

→ Using low-latency DEM with switch matrix



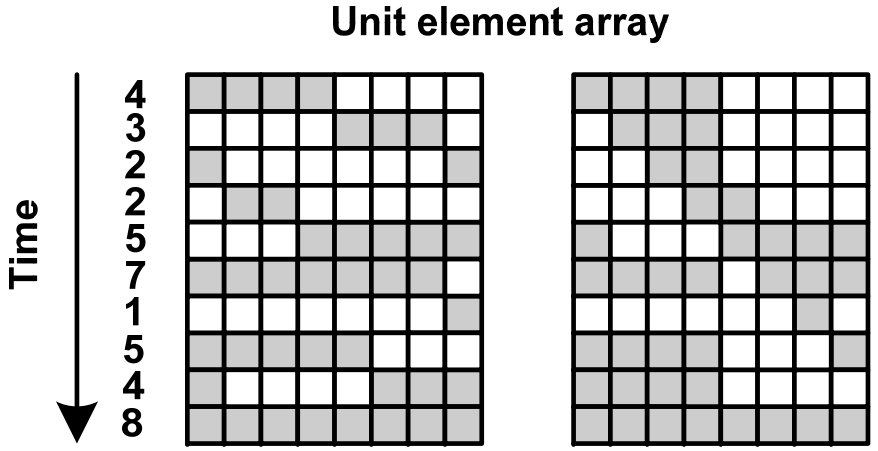
Conventional DEM



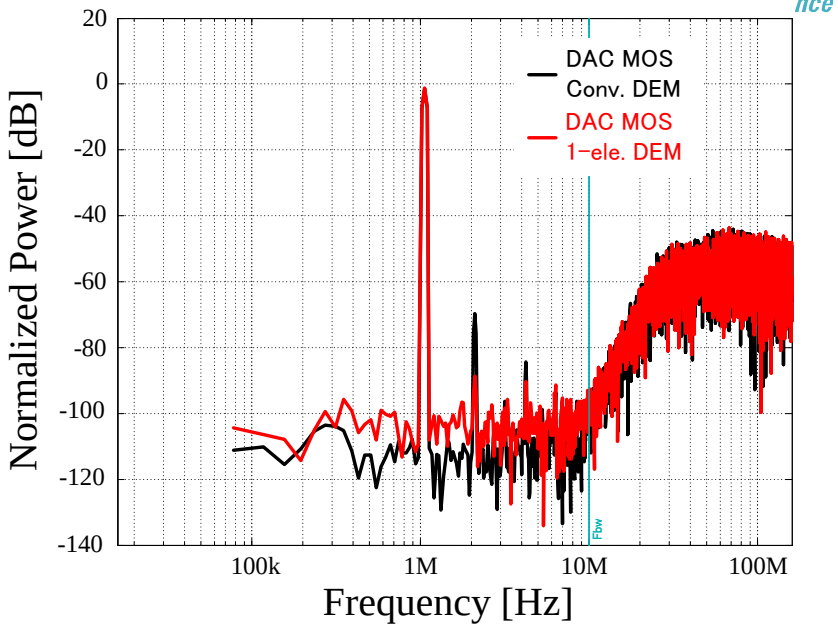


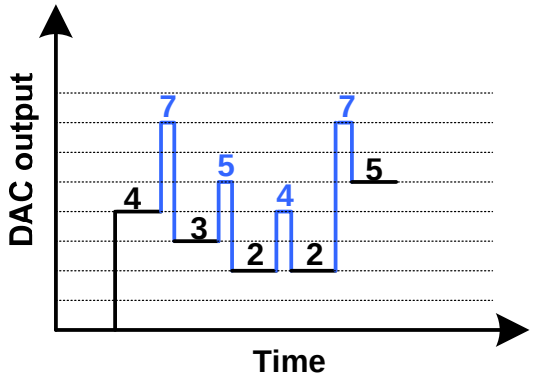
Increase of DAC output glitch

Proposed 1-element shifting DEM

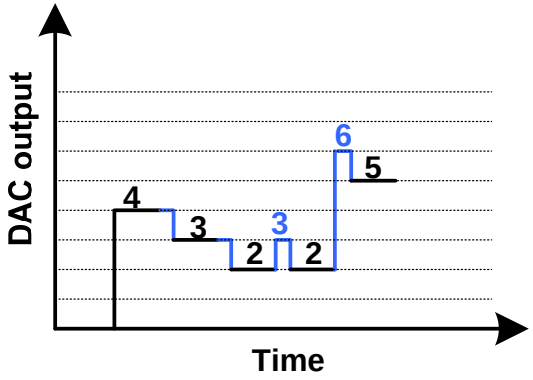


Conventional DEM　　1element DEM





Conventional DEM

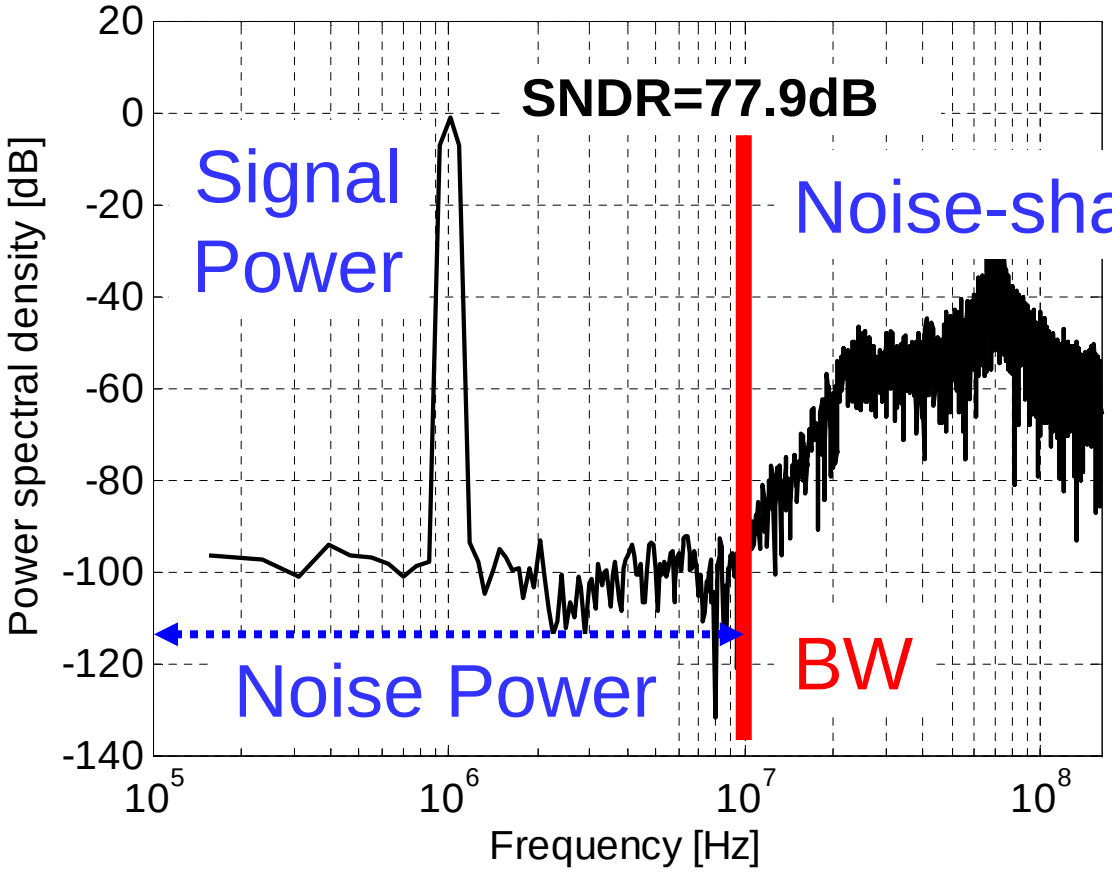


1element DEM

	Conv. DEM	1−ele DEM
Resolution	68dB	81dB
Area Power Delay	Almost same	

Relax DAC output glitch

Simulation result



8.1 mW @

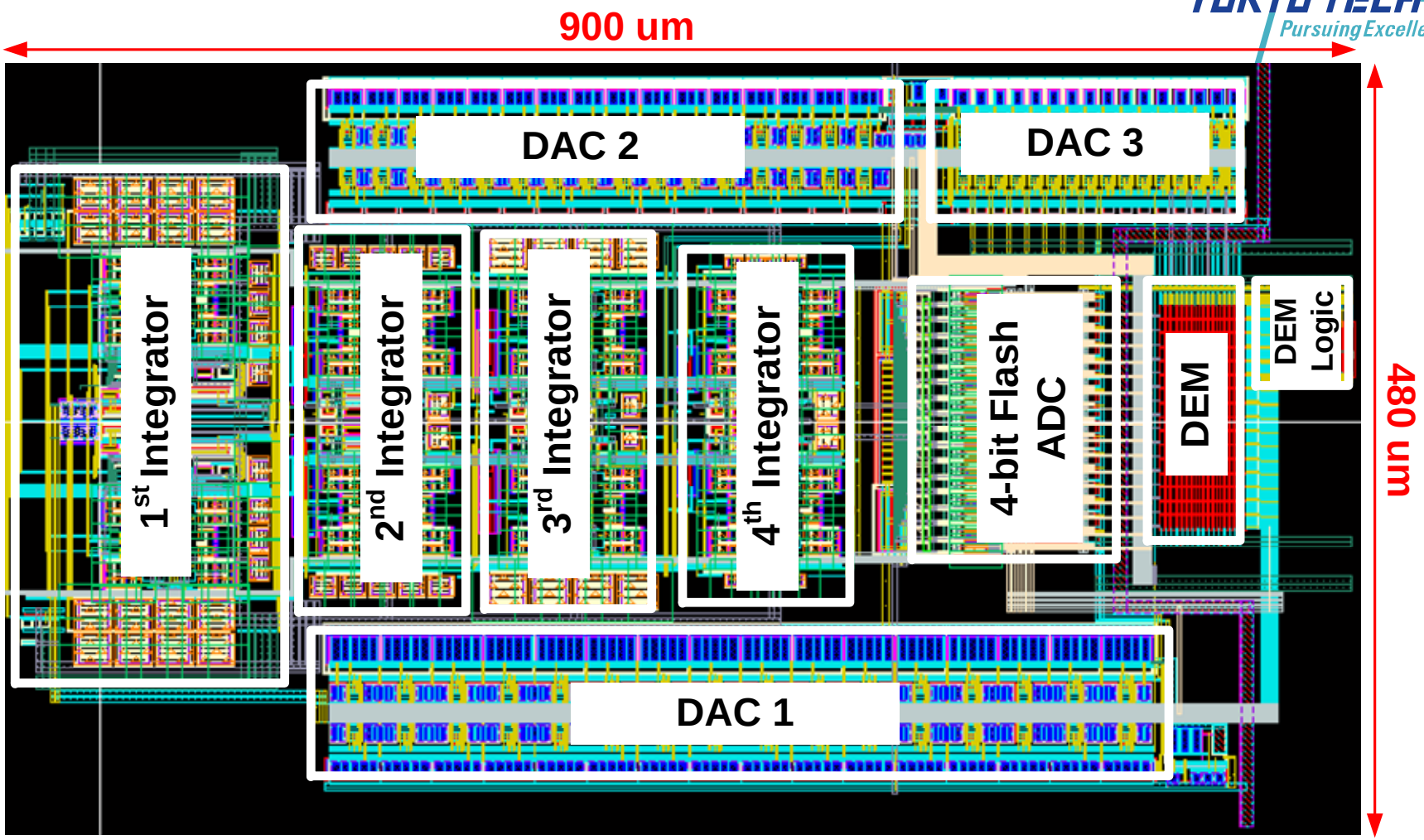
-1 dBFS

SIM condition

- **All blocks in transistor level**
- **Without noise because of huge SIM time**
- **Without mismatch (SIM time)**

} **Confirmed in small level with some ideal blocks**

Modulator layout



Layout core size : 900 um x 480 um

(90nm CMOS process)

Modulator performance

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Bandwidth	10MHz
Sampling frequency	320MHz
Resolution (simulation)	77.9dB
Input range	1.6V diff
Supply voltage	1.2V
Power consumption (simulation)	8.1mW
Area	0.9 x 0.48 mm^2
Process	90nm CMOS process
FoM (simulation)	62fJ/conv

According to the proposed low power, low noise OPAMP, good FoM is estimated.

Performance comparison (1)

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SNDR [dB]	Power [mW]	FoM [pJ/conv]	BW [MHz]	Fs [MHz]	Supply [V]	Reference
77	**8.1**	**0.07**	**10**	**320**	**1.2**	**This work (SIM)**
74	20	0.12	20	640	1.2	ISSCC 2006 3.1
72	28	0.22	20	420	1.2	ISSCC 2008 27.5
66	7.5	0.23	10	600	1.8	ISCAS 2006
62.5	5.32	0.24	10	300	1.1	VLSI 2009
60	10.5	0.32	20	250	1.3	ISSCC 2009 9.7
78.1	87	0.33	20	900	1.5	ISSCC 2009 9.5
68.8	42.6	0.41	23	276	1.8	ISSCC 2005 27.6
79	75	0.43	12	240	2.5	ISSCC 2003 23.6
82	100	0.49	10	640	1.8	ISSCC 2008 27.6
69	56	0.61	20	340	1.2	ISSCC 2007 13.1

$$FOM\,(pj/conv) = \frac{Power}{2^{ENOB} \times 2 \times signalband}$$

(Smaller FoM is better)

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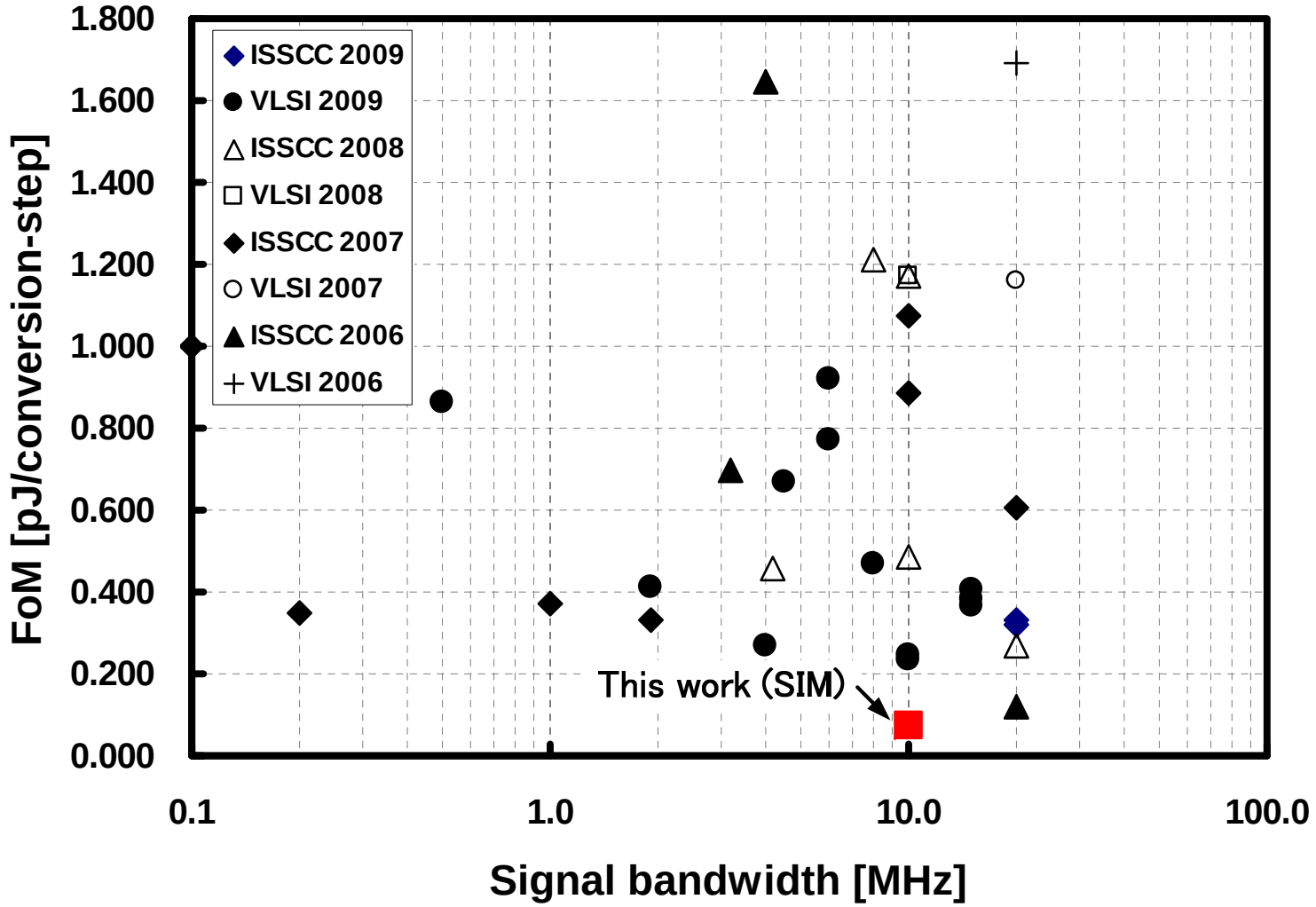
Performance comparison (2)



Best FoM value is expected (simulation)

Conclusion

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- A low power, low noise OPAMP is proposed.
- A 10MHz BW $\Delta\Sigma$ ADC is designed for Software Defined Radio in 90nm CMOS process.
- Simulation results obtain 77.9dB SNDR at 8.1mW power consumption. According to proposed low power, low noise OPAMP, best FoM at 62fJ/conv is expected.

Acknowledgement

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Reference

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[7] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa, “A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs,” *ASSCC Dig. Tech. Papers*, pp. 269-272, Nov. 2008.

[8] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx,“An 820mW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS,” *ISSCC Dig. Tech. Papers*, pp.238-239, Feb. 2008.

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Thank you for your kind attention!

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